Novel MIC Bipolar Frequency Doublers Having High Gain, Wide Bandwidth and Good Spectral Performance

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Abstract—**New high efficiency Bipolar microwave frequency multipliers have been developed having wideband performance, high conversion gain and good spectral properties. Experimental conversion gains of up to 7 dB have been attained for narrow bandwidths ($\approx 8\%$) and approximately 0 dB for wide-band designs (40%) at *C* band. Corresponding fundamental and 3rd harmonic rejections are greater than 40 dBc. Extensive modeling and computer-oriented design have been employed utilizing harmonic balance.**

I. Background

FREQUENCY multiplying circuits find broad application in electronic systems operating in the RF and microwave frequency ranges. Such devices are employed to provide improved design flexibility and transmitter capability in CW, AM and FM transmitter systems and, in the case of low power systems, for application in local oscillators and frequency synthesizers. Low noise frequency multiplication is also highly desirable for modern wideband phase-locked sources for high frequency system applications.

Recently, considerable attention has been focused on the development of high frequency active multipliers using GaAs FET's [1]–[15]. The development of such multipliers is being pursued since they provide the possibility of conversion gain over a broad band of frequencies, have isolation between output and input terminals, and possess good efficiency in comparison with their diode counterparts. FET multipliers are also investigated because of their potential for lower noise operation, although apparently there has not as yet been a definitive study on this topic [16].

These FET designs feature methods for providing high conversion gain at higher frequencies with typical results (for the fundamental multiplying element) frequently less than 0 dB [1], [8], [9], [13], [15], although some designs provide gains of several dB. Except for several special situation designs [5], [10] typical reported bandwidths are on the order of 5–10% with 20% being reported in one case [1]. Unwanted frequency components at the output of multiplier circuits constitute another area of concern which has frequently not been given great attention. Indeed, a perusal of the literature on FET multipliers reveals in many cases, that the rejection of the fundamental frequency component at the multiplier output is frequently not as great as desired.

This paper presents the theory and design of new and unique bipolar frequency doublers which have high gain, wide bandwidth and good spectral performance (i.e., regarding fundamental and undesired output harmonics). The designs feature the use of a bipolar Darlington pair MMIC as the nonlinear element embedded in passive matching networks to provide narrowband designs (8–12%) with up to 7 dB conversion gain and wide-band (40%) designs with approximately 0 dB conversion gain at *C* band. These designs possess fundamental and 3rd harmonic suppressions greater than 40 dBc.

The fact that a Darlington pair was used as the multiplying element makes this research different from all previous work in this field. Darlington pairs are most widely known for their high current gain and high input impedance in linear amplifier applications. However, a particular configuration of the Darlington pair designed and fabricated in integrated circuit form by Avantek, Inc. [17] has been found to have some very appealing nonlinear properties [18] which will be discussed below in Section II.

II. Nonlinear Device Description

The device employed as the nonlinear element for the multiplier design is the Avantek MSA-08 silicon bipolar monolithic microwave integrated circuit (MMIC) [17] (referred to as A08 in the remainder of this paper). The A08 (Fig. 1) is a traditional Darlington pair with an integrated, three-resistor bias network that allows the device to be biased by a single positive supply through an external resistor and RF choke. Originally designed for use in linear amplifier applications, it can provide gain in excess of 32 dB below 100 MHz and has useable gain slightly above 6 GHz. The power handling capability of the A08 is indicated by its 1 dB compression point. At 2 GHz, the 1 dB compressed output power is approximately 12 dBm for a 36 mA bias. A large signal model of the A08 was

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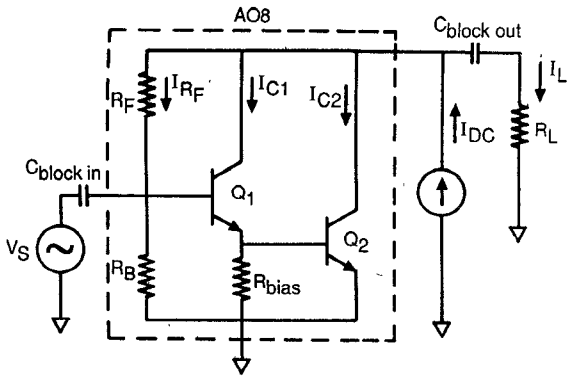

Fig. 1. Circuit diagram showing branch circuits.

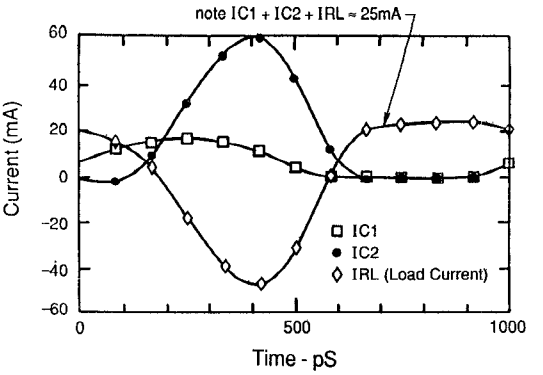

Fig. 2. Simulation of A08 collector currents and current through a 50 Ω load. Bias = 25 mA, input power = 0 dBm; frequency = 1 GHz.

developed specifically for this work [19] to gain a better understanding of the device behavior. The model, which accurately predicts gain compression and harmonic generation in a 50 Ω system over a limited range of biases, was used for the simulations presented later in the paper.

The circuit diagram in Fig. 1 can be used to explain the operation of the A08 under large input signal conditions. The capacitors on input and output serve only to block dc current and can be assumed to be short circuits for time-varying signals. The branch currents which are shown represent a superposition of dc and large signal ac components. The dc bias current source has been included so that KCL can be applied to the output node. Since the resistor R_F is large enough that the current through it is small compared to the other four currents, I_{RF} is neglected in applying KCL so that we may write

$$I_{dc} = I_{C1} + I_{C2} + I_L. \tag{1}$$

Since I_{dc} is constant, the operation of the device is intuitively obvious: a large sinusoidal voltage at the device input periodically turns Q_1 on and off so that I_{C1} has the form of a rectified sine wave. When Q_1 is turned on, the collector current shows up in the emitter to turn Q_2 on, and when Q_1 is turned off, there is no emitter current so Q_2 must be turned off as well. Consequently, I_{C2} has the form of a rectified sine wave. However, I_{C2} is out of phase with I_{C1} because of the delay introduced by the necessity to store or extract minority charge in the base of Q_2 before it can be turned on or off respectively. Since the sum of the three currents on the right side of (1) must always be constant, it is clear that when Q_1 and Q_2 are turned on hard, their collectors must pull a large amount of current from the load (I_L is negative). Conversely, when both Q_1 and Q_2 are turned off, all of the dc source current must be forced through the load (I_L is positive, and equal to I_{dc}). Q_2 is 2.8 times larger than Q_1 and it has a higher quiescent operating current; it therefore stands to reason that Q_2 has a much larger influence on the load current than Q_1. For example, when Q_2 is turned on hard, its peak collector current is as much as four times larger than the peak collector current of Q_1. For this reason, the distortion in the output current is due primarily to the distortion in I_{C2}.

The above analysis applies well when the excitation frequency is relatively low (below 1 GHz). However, at higher frequencies, other effects must be taken into account. For example, the simple diagram in Fig. 1 does not include parasitic capacitances which must be charged and discharged during the rapid transitions when Q_1 and Q_2 go from off to on and on to off respectively. The resulting currents make (1) inaccurate during the transitions. Fig. 2 shows a simulation of the two collector currents and the load current for an A08 at 25 mA bias, driven by a 0 dBm input signal at 1 GHz. Note that away from the transitions the sum of the three currents is approximately equal to the 25 mA bias current. Note also that the load current is dominated by the I_{C2} contribution.

One of the peculiarities of the Darlington configuration as compared to a common-collector common-emitter (CC-CE) connection is that the collector node of the input transistor is connected directly to the output node. This leaves a direct feedback path from output to input through the collector-base junction capacitance of the first transistor. This feedback path may be responsible for observed sensitivity of conversion gain on input termination at the second harmonic frequency. In a doubler application, the large second harmonic signal generated at the A08 output is fed back to the device input through the junction capacitance. As will be discussed in Section III, the second harmonic signal at the device input can be reflected back into the device by the presence of an appropriate input network, thus resulting in a large improvement in conversion gain.

III. Multiplier Design

In this section the specifications that were applied to the Darlington doubler and the design methodology used to achieve them are described. The overall goal was to develop a design philosophy for bipolar doublers that exhibit good conversion gain (> 0 dB), good rejection of fundamental, third, and higher harmonics (at least 40 dBc), and flat frequency response in a 50 Ω system. These specifications should provide a general purpose frequency doubler that is of practical value. If a designer

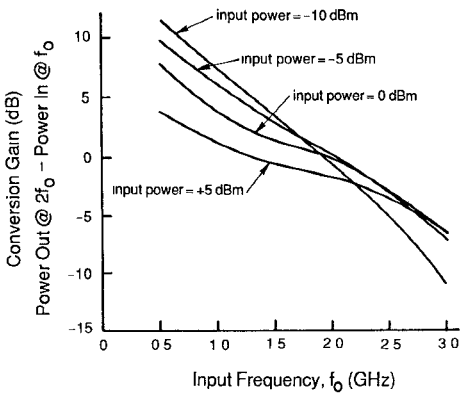

Fig. 3. Measured conversion gain of A08 for different input power levels (50 Ω input and output terminations, 20 mA bias).

had a specific application for which a comparable doubler could be used, particular attention could be paid to achieving better performance in certain specifications, perhaps at the cost of less than optimal performance in others.

In practice, there is an additional set of design specifications which would dictate, or at least constrain, the choice of nonlinear device and substrate materials. Such specifications include: operating frequency, power dissipation, noise performance, input drive level, and physical size. In this case, since the nonlinear device was chosen *a priori*, the specifications were constrained instead. With regard to noise, no effort was made to design for, or even measure, noise performance. The other specifications are discussed below.

Operating Frequency: As found in TVRO applications, the center output frequency ($2f_o$) was chosen as 4 GHz. This frequency was high enough to make the design sufficiently challenging, while at the same time offering the potential of obtaining significant conversion gain. Preliminary measurements indicated that the conversion gain of the A08 in a 50 Ω system (50 Ω source and load impedance) dips below 0 dB for fundamental inputs above 2 GHz (see Fig. 3).

Input Drive Level: Characterization of an A08 in a 50 Ω system indicated that highest conversion gain for inputs in the 2 GHz range is obtained for input powers between −5 and 0 dBm. However, Fig. 3 indicates that an A08 doubler could operate with reasonable performance for input powers in the range of −10 to +5 dBm.

Power Dissipation: The amount of dc power dissipation of the final doubler design was given only minor consideration. Preliminary measurements of the A08 indicated that the highest conversion gain would be achieved for supply currents in the neighborhood of 20–25 mA. Since the output node (where the current is supplied) is nominally about 7.7 V dc, the corresponding power dissipation is only about 170 mW. While this might be significant when compared to a FET multiplier biased in cutoff (zero quiescent drain current), it is small compared to the power dissipated in typical microwave analog IC's.

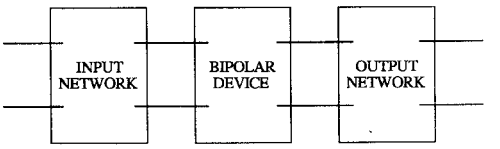

Fig. 4. Network configuration.

Stability: The standard topology for many multiplier circuits is shown in Fig. 4. The nonlinear device chosen for this work was described in the previous section; the remainder of this section is devoted to discussion of the input and output networks. The strategy which resulted in the final doubler circuit was to first synthesize an output network which optimally terminated the A08 for conversion gain and rejected unwanted harmonics; and second, to develop an input network which enhanced conversion gain by improving input match and/or reflecting second harmonic back at the device input. As the two networks were designed independently, they are discussed separately below. The topic of stability is included with the discussion of the output network since the design of the output network is greatly constrained by the need to make the final circuit unconditionally stable.

Output Network

The doubler output network has two major functions: first, to terminate the nonlinear device in such a way as to maximize the generation of second harmonic; second, to pass the second harmonic while attenuating the fundamental and all other unwanted harmonics. We begin by discussing the effect of fundamental termination on harmonic generation.

As described in Section II on the operation of the A08, the primary source of distortion (harmonic generation) comes from the nonlinear action that occurs when the two transistors switch from cutoff to forward-active operation. If that action can be enhanced in some way by the device termination, higher harmonic power can be generated. Regressing for a moment, recall from the A08 description in Section II that the load current can be roughly approximated as the source current minus the sum of the two collector currents. Now, with sufficiently high input power, the two transistors turn on and off for a portion of the cycle, and, neglecting other distortions, the collector current waveforms can be approximated to first order as partially rectified cosine waves as shown in Fig. 5, where the conduction angle, θ, is defined as the portion of the cycle over which the devices are turned on. The load current is a combination of two such waveforms: one from the Q_1 collector current and one from the Q_2 collector current. As mentioned earlier, I_{C2} has a larger amplitude and it lags behind I_{C1}. The Fourier series of the I_{C1} waveform is given by

$$I_{C1} = a_0 + \sum_{n=1}^{\infty} a_n \cos(n\omega_0 t) \tag{2}$$

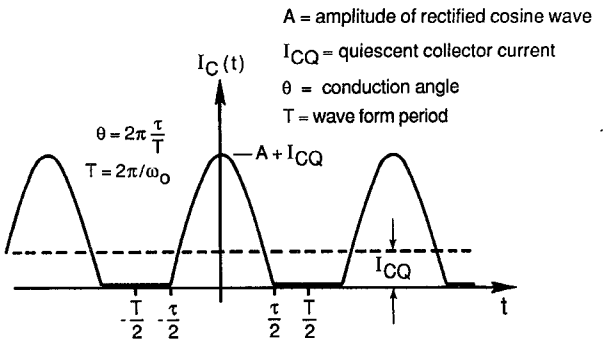

Fig. 5. Collector current waveform approximated by a partially rectified cosine wave.

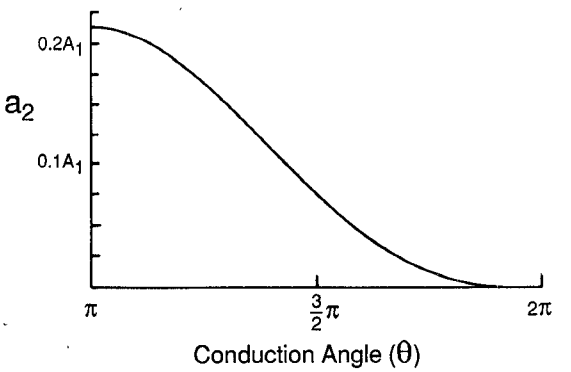

Fig. 6. Amplitude of second harmonic component of rectified cosine wave as a function of conduction angle.

where

$$\omega_0 = \frac{2\pi}{T}$$

$$a_0 = I_{CQ_1} + \frac{A_1}{\pi}\sin\left(\frac{\omega_0\tau}{2}\right) + \frac{A_1(T-\tau)}{T}\cos\left(\frac{\omega_0\tau}{2}\right)$$

$$a_n = \frac{A_1}{\pi}\left[\frac{\sin[(n+1)\omega_0 t/2]}{n+1} + \frac{\sin[(n-1)\omega_0 t/2]}{n-1}\right] - \frac{2A_1}{n\pi}\cos\left(\frac{\omega_0 t}{2}\right)\sin\left(\frac{n\omega_0 t}{2}\right).$$

If we assume that the I_{C2} waveform is similar to that of I_{C1} with a different amplitude A_2, and a phase shift ψ, the Fourier series for I_{C2} can be written as

$$I_{C2} = b_0 + \sum_{n=1}^{\infty} b_n \cos[n(\omega_0 t - \psi)] \tag{3}$$

where

$$\left.\begin{aligned} b_0 &= a_0 \\ b_n &= a_n \end{aligned}\right\} \text{ with } I_{CQ_1} \text{ replaced by } I_{CQ_2} \text{ and } A_1 \text{ replaced by } A_2.$$

For simplicity, the conduction angles are assumed equal.

Assuming that all unwanted components, including dc, can be effectively filtered so that the load current will contain only second harmonic, the load current waveform can be obtained from (2) and (3):

$$I_L = a_2 \cos(2\omega_0 t) + b_2 \cos[2(\omega_0 t - \psi)] \tag{4}$$

where

$$a_2 = \frac{A_1}{\pi}\left[\frac{1}{3}\sin\left(\frac{3}{2}\theta\right) + \sin\left(\frac{1}{2}\theta\right) - \cos\left(\frac{1}{2}\theta\right)\sin(\theta)\right]$$

$$b_2 = \frac{A_2}{\pi}\left[\frac{1}{3}\sin\left(\frac{3}{2}\theta\right) + \sin\left(\frac{1}{2}\theta\right) - \cos\left(\frac{1}{2}\theta\right)\sin(\theta)\right].$$

As mentioned above, one of the goals in the design of the output network is to maximize the amplitude of the second harmonic current in the load resistor. In the above equation, there are several parameters that can be controlled to accomplish this: the conduction angle, θ, and the amplitudes of the collector current waveforms, A_1 and A_2. The angle ψ should ideally be minimized so that the two components add perfectly in phase; however, ψ is related to the propagation delay through Q_2, and we have little control over this parameter.

First, we examine the effect of the conduction angle, θ. The magnitude of a_2 is plotted as a function of θ in Fig. 6. Clearly, the optimum conduction angle is π radians. As the conduction angle approaches π, the second harmonic amplitude reaches a maximum. Conduction angles less than π can only be achieved if the devices are biased in cutoff. By examining Fig. 5, it is seen that one way of making the conduction angle closer to π is by decreasing the quiescent collector current I_{CQ}. There is a trade-off involved, however, because the transistor's gain (and thus the amplitude of the collector current waveform) decreases as the quiescent current is decreased. Another way of making the conduction angle more optimal is by increasing the amplitude of the dynamic collector current, and thus increasing the slope of the waveform near the region where it becomes cutoff. To a certain extent, this can be accomplished by increasing the amplitude of the driving signal. But once again, there is a trade-off involved, because the device gain (both linear gain and conversion gain) begins to compress once the input power is increased beyond a certain level and different nonlinearities become more important.

Now, consider the amplitudes, A_1 and A_2, of the collector current waveforms. One way of increasing the peak collector current amplitude of Q_2 is by presenting the device output with a low impedance load at the fundamental frequency. In order to show that this is true, it is necessary to examine how the load impedance affects the dynamic load line for Q_2, and thus the collector current waveform. Fig. 7 shows high impedance and short circuit load lines superimposed on the I_C versus V_{CE} characteristic curves for a common-emitter transistor. There are two important qualitative characteristics to notice in this figure. The first and most striking is the way that the peak collector current amplitude can be signifi-

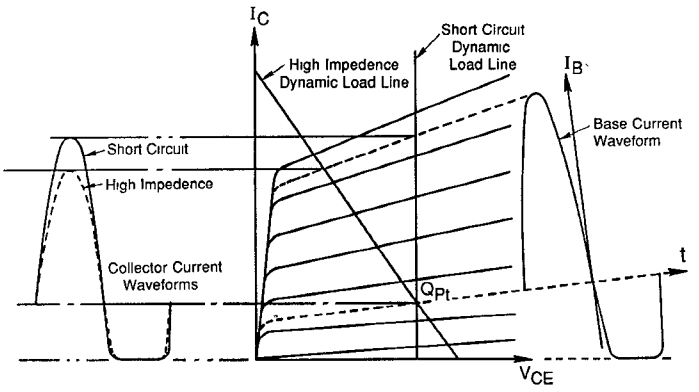

Fig. 7. Load line analysis showing the effect of load impedance on output current amplitude.

cantly increased by increasing the slope of the load line due to the Early effect of the transistor (positive slope of the I_C versus V_{CE} curve in the forward active region). The second, less obvious characteristic is the way in which the conduction angle is smaller for the short circuit load. As mentioned in the preceeding paragraph, the reduced conduction angle is due to the increased slope of the collector current waveform in the region where it becomes cutoff.

The transistors in the IC process used to produce the A08 have a low Early voltage (on the order of 20 V); this may be attributable to the necessity of making the base region extremely narrow to reduce base transit time, and thus achieve high frequency performance. Therefore, the output current waveform of the A08 is particularly sensitive to the load impedance as indicated in Fig. 7. The above analysis suggests that the optimum terminating impedance for second harmonic generation is a short circuit at the fundamental frequency. This conjecture is supported by computer simulation, and by actual experimental results that will be described in Section IV.

Now that the termination at the fundamental frequency has been discussed, the terminations at other harmonics must be considered. Obviously, since the second harmonic is the desired frequency component, we would like the maximum power transferred to the load at this frequency. Thus, the required termination for optimum conversion gain is a conjugate match to the A08 output impedance. Determination of the optimum termination impedances at the third and higher harmonics is very difficult and (judging from the small amount of attention that this topic is given in the literature) commonly neglected by most doubler designers. Two authors briefly mention the topic [9], [10], [12]; both of them state only that unwanted harmonics should be terminated reactively to prevent power loss in them, and that the reactance should be chosen to enhance the output power in the desired harmonic. The mechanism by which higher harmonic terminations affect the output at the desired harmonic is somewhat complicated. Unwanted harmonics reflected back into the device from the output network are mixed together with other frequency components by the device nonlinearities. Some of the mixing products (i.e., $3f_o - f_o$) will be at the same frequency as the desired output signal and will either add to or subtract from it. Whether the interference is constructive or destructive depends on the phase at which the higher harmonic is reflected back into the device, and this in turn is determined by the reactance of the termination. As a practical matter, the design of an output network that could realize the optimum terminating reactances (which would have to be determined empirically) over any sort of bandwidth while simultaneously meeting filtering and other constraints would obviously be very difficult. For this reason, optimization of higher harmonic terminations was not attempted.

The other function of the output network, that of rejecting unwanted frequency components, is now considered. Clearly, some type of filter network is required, and preferably one that presents a short circuit (or approximately so) to the A08 output over the fundamental frequency bandwidth. There are several possible synthesis approaches that can be employed. One approach is to specify exactly the desired frequency response of the output network subject to physical realizability constraints, and then use exact synthesis techniques and an optimizing program to construct a network that approximates the specified response. A second approach is to make use of modern filter theory to design a conventional filter that has most of the desired characteristics. Since there are straightforward procedures available for the design of distributed filters, the latter approach is simpler and was adopted in this paper.

The desired filter response is bandpass, with the pass band centered about the second harmonic. The passband ripple should be kept small to preserve the flatness, and the out of band rejection should be high enough to achieve the 40 dBc specification (i.e., fundamental and all undesired harmonics should be 40 dB below the desired output signal). The required steepness of the filter roll-off depends on the bandwidth of the design; a 40% bandwidth design would require a filter with infinitely steep roll-off since the lower edge of the third harmonic band would be the same as the upper edge of the second harmonic band. Standard filter synthesis techniques re-

quire that both filter terminating impedances be real. Obviously, the output impedance of the A08 is not purely real, but it is "close" to 50 Ω (VSWR < 1.5:1) in the 3–5 GHz frequency range (output band). So, the approach used for the output filter was to assume that the A08 had a 50 Ω output impedance. It should be noted that large signal impedances could ideally be used for the design of matching networks; however, equipment was not available to make such measurements. For this reason, small-signal s-parameters were used as an approximation of the large signal impedances.

As alluded to earlier, stability plays a very important role in the choice of the terminating networks since the A08 is not an unconditionally stable device. Therefore, care must be taken to ascertain that the impedance presented to the A08 by the output network does not result in a negative resistance at any frequency at the input of the device. Fig. 8 shows several stability circles for the output of an A08. In this case, the regions inside of the circles represent stable terminating impedances at the frequencies for which the circles are drawn. Unfortunately, the upper portion of the Smith chart (inductive reactances) is off limits at low frequencies. This means that the output network must be chosen carefully such that its input impedance follows a trajectory along the bottom edge of the Smith chart at low frequencies, and then loops in towards the center of the chart (50 Ω) in the second harmonic band.

Observation of Fig. 8 shows that the desired short circuit (the leftmost point on the chart) termination falls in an unstable region of the Smith chart at 2 GHz. Therefore, the best approach is to come close to a short circuit termination in the fundamental band, with the lower frequency terminations being further from the ideal. Since short circuits and inductive reactances are unacceptable at low frequencies, a design which utilizes short circuited stubs directly coupled to the A08 output cannot be used; this eliminates a complete class of filter topologies. The alternative is to use a filter topology which presents an open circuit to the A08 at low frequencies. Then a short section of series transmission line can be used to provide additional phase shift to move the fundamental band termination closer to the optimum. This is demonstrated in Section IV.

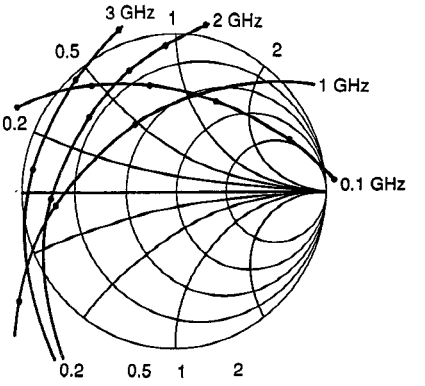

Fig. 8. Output stability circles for A08 (bias = 25 mA). Inside region represents stable terminating impedances at frequency for which circle is drawn.

Input Network

In the present design approach, the doubler input network has three major purposes: it should enhance rather than degrade the overall conversion gain of the doubler, it should attenuate harmonic frequency components that are reflected back at the source, and finally, it can also be used for improving input VSWR.

The first and second purposes of the input network are intimately related, and therefore will be discussed together. The input impedance of the A08 is strongly influenced by the nonlinearity of the Q_1 base-emitter diode. Due to this nonlinearity, the input impedance is both frequency and voltage dependent. Thus, the input current is distorted under high input drive levels, resulting in a distorted voltage across the linear source impedance. So, harmonic signals generated at the device input are effectively reflected back towards the source.

Experimental results show that there is significant harmonic power reflected back to the source, and that the amplitude of the reflected power is strongly dependent on the A08 output termination. In order to utilize this effect, the input network should be designed to re-reflect harmonic signals back into the A08 input. However, this must be accomplished with considerable caution since the re-reflected signals can be linearly amplified by the A08 or intermodulated with the fundamental signal, causing unpredictable results. Obviously, depending on their phases, the re-reflected signals can interfere either constructively or destructively with the desired output signal after propagating through the A08. It is thus desirable to have re-reflected signals incident in such a way as to maximize conversion gain. But, because of the complicated nature of the interference, a suitable input termination is most easily determined empirically either by experimentation or by multiple simulations with an accurate nonlinear model. Computer simulations at a single frequency (2 GHz fundamental) have suggested that the conversion gain could be enhanced by as much as 5 dB, or degraded as much as 8 dB, depending upon the phase of the re-reflected second harmonic signal.

IV. Performance of Experimental Doublers

Narrow, medium, and wide-bandwidth doublers with output center frequencies of 4 GHz have been developed and fabricated on low-loss teflon-fiberglass circuit board utilizing input and output networks composed solely of microstrip elements. The narrow-bandwidth doublers, designed to operate at a single frequency, were used to experimentally characterize the effect of fundamental output termination on conversion gain. These designs verified the hypothesis that a short circuit provides the optimum fundamental termination, and also gave valu-

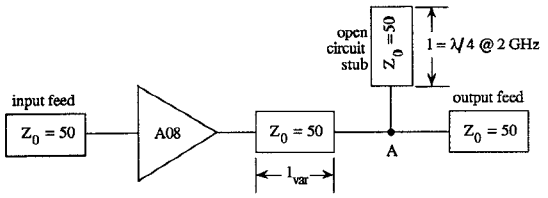

Fig. 9. Schematic of narrowband circuit.

able information about how the conversion gain behaves as the fundamental termination becomes less optimum.

Medium-bandwidth designs were fabricated with and without input reflector networks. A conversion gain improvement of nearly 7 dB was attained when a network was added to reflect second harmonic back into the A08 input at the optimum phase. A wide-bandwidth design which did not include an input reflector network achieved a flat conversion gain of approximately 0 dB. The output networks of all designs incorporated bandpass structures to reduce the fundamental and third harmonic levels at the doubler outputs.

Narrowband Designs

The narrowband designs consist of a short section of 50 Ω transmission line for an input feed network, an A08, a second length of 50 Ω transmission line, a quarter wavelength (@ 2 GHz) 50 Ω open circuit shunt stub, and a length of 50 Ω line for an output feed. The circuit is shown schematically in Fig. 9. The quarter wavelength open stub presents a short circuit to node A in Fig. 9 at 2 GHz, and an open circuit to node A at 4 GHz. Thus, the stub ideally has no effect on the second harmonic output termination at 4 GHz. The fundamental frequency termination was altered by changing the line length l_{var} between 1/2 and 1/4 wavelength at 2 GHz. When l_{var} is 1/2 wavelength long, the A08 output sees a short circuit fundamental termination. As l_{var} is shortened, the termination moves counter-clockwise around the outside edge of the Smith chart (purely reactive); at 1/4 wavelength, the A08 output sees an open circuit fundamental termination. Eight circuits were constructed with l_{var} varying between 1/2 and 1/4 wavelength in order to measure the effect of a variety of fundamental load terminations with a constant 50 Ω second harmonic termination.

Each circuit was measured at a single representative bias point (25 mA) and a single input power (0 dBm) to verify the relation between conversion gain and terminating impedance. The results of these measurements are summarized in Fig. 10 where conversion gain is plotted as a function of the phase at which the fundamental is reflected back toward the A08 output (−180° in the short circuit case, and 0° in the open circuit case). This is a particularly convenient form in which to present the data because the phase on the horizontal axis is just the angle of the output network fundamental frequency reflection coefficient Γ, which is defined by

$$\Gamma = [(Z_1 - Z_0)/(Z_1 + Z_0)],$$

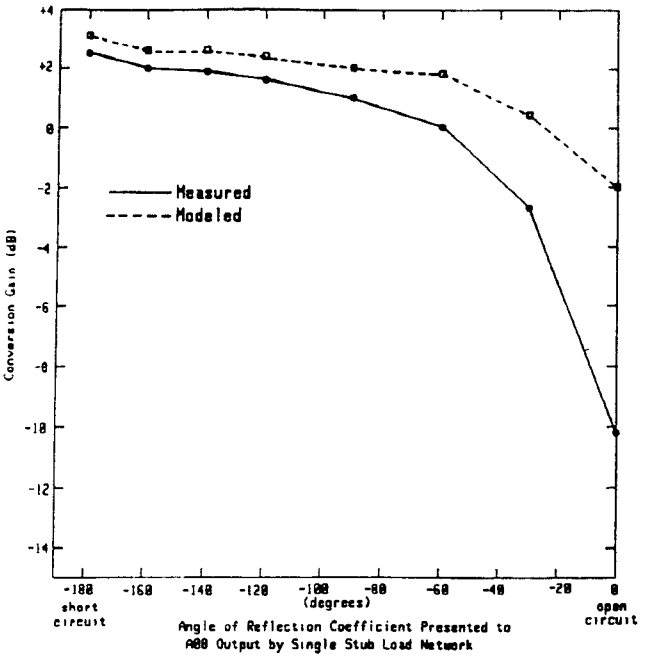

Fig. 10. Conversion gain of narrowband doubler as a function of the phase of the load reflection coefficient (bias = 25 mA; input power = 0 dB; frequency = 2 GHz).

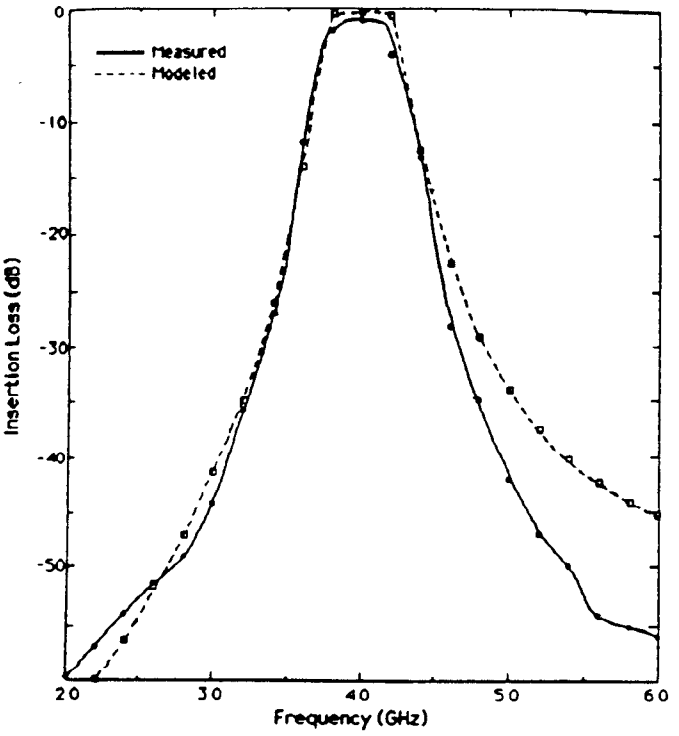

Fig. 11. Measured and modeled insertion loss of edge-coupled filter used in medium band doubler designs.

where Z_1 is the load impedance at the fundamental frequency and Z_0 is the reference impedance (50 Ω). Thus, this plot can be used to estimate the conversion gain (at 2 GHz) for future doublers (without input networks) from the knowledge of Ang(S_{11}) of the output network. This assumes that $|S_{11}|$ is near unity, which it

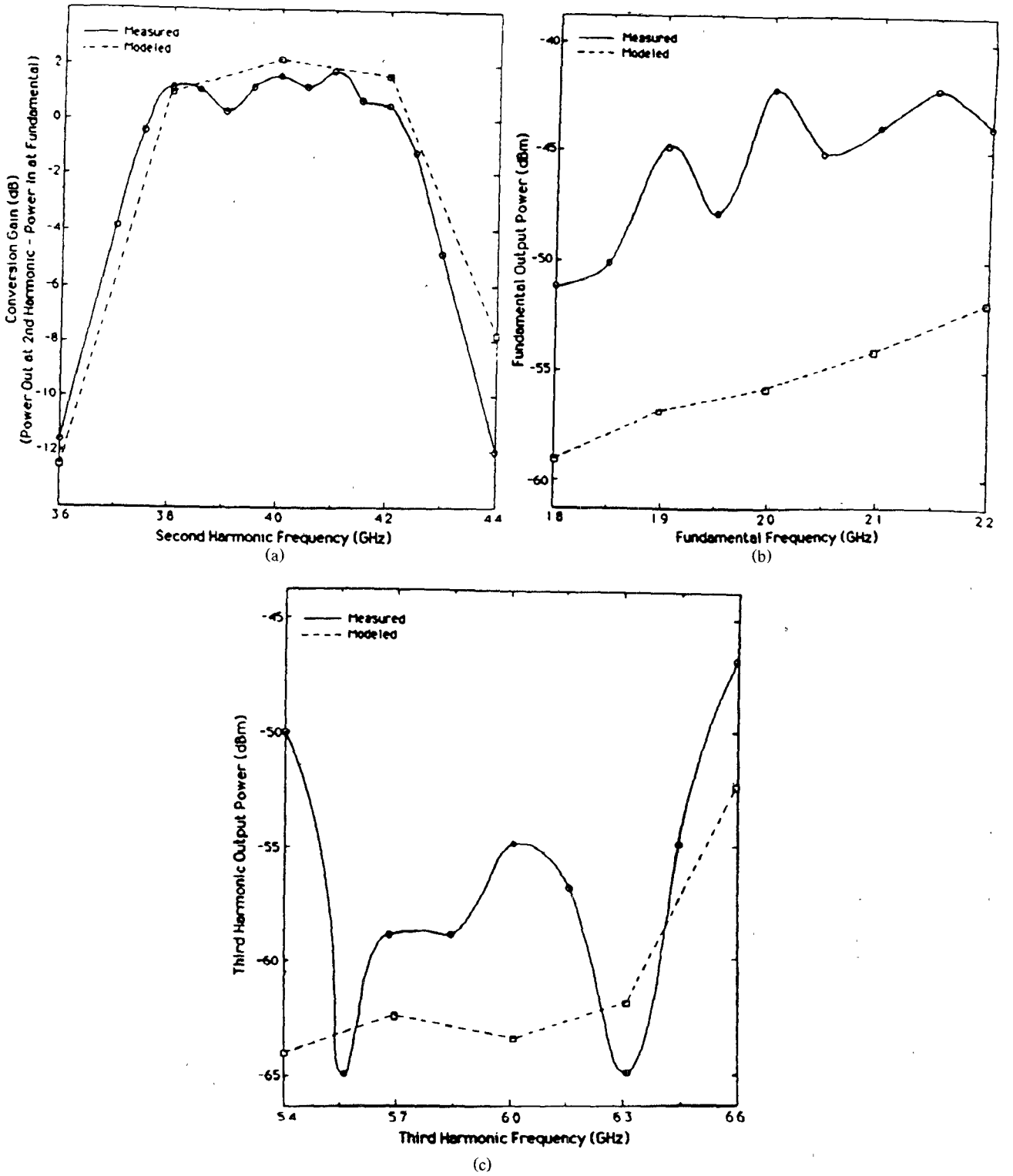

Fig. 12. (a) Measured and modeled conversion gain of medium band design #1. Bias = 25 mA; input power = 0 dBm. (b) Measured and modeled fundamental output power of medium band design #1. Bias = 25 mA; input power = 0 dBm. (c) Measured and modeled third harmonic output power of medium band design #1. Bias = 25 mA; input power = 0 dBm.

must be in order to keep the fundamental power dissipated in the load resistor to a minimum.

Although the modeled data exhibits the correct trend, the difference between the measured and modeled data in Fig. 10 becomes quite substantial (8 dB) as the termination impedance approaches an open circuit. Most of the discrepancy can be attributed to inaccuracies in the model. As characterized in Fig. 10, the important outcome of the narrowband analysis is the demonstration of the manner in which conversion gain is affected by the angle of the reflection coefficient of the output network at the fundamental frequency: over the range of angles

from $-180°$ to $-60°$, the conversion gain gradually decreases by about 2 dB; for angles more positive than $-60°$, the conversion gain falls off rapidly.

Medium Bandwidth Designs

It may be recalled from the previous section that the first step of the design approach was to ascertain a standard filter topology that approximated the desired output termination. A particular "medium" bandwidth filter topology that is widely used is the edge-coupled bandpass filter. This topology provides a purely capacitive termination for dc and frequencies well below the passband. For this reason, it is believed to be ideal for providing a stable termination to the A08 in the doubler application.

A design for a theoretical doubler bandwidth of 13.5% was developed utilizing an 0.1 dB Tchebycheff response. Since the desired doubler bandwidth was relatively narrow, a third order design provided sufficiently fast roll-off that the fundamental and third harmonic bands were properly attenuated.

The measured and theoretical insertion loss of the filter are shown in Fig. 11. The input impedance of this filter follows a clockwise trajectory with increasing frequency along the bottom edge of the Smith chart. At the 2 GHz center of the fundamental band, the angle of the input reflection coefficient is approximately $-90°$. It is clear from Fig. 10 that this is a suboptimum termination for maximum conversion gain. The termination can be made closer to the optimal value ($-180°$) by inserting a short length of transmission line in cascade with the filter input. It is important, however, that the transmission line is short enough such that it does not rotate the impedance trajectory into an unstable region of the Smith chart (see Fig. 8).

The first circuit fabricated using the edge-coupled filter incorporated a 300 mil length of 50 Ω transmission line (resulting in approximately 50° of clockwise rotation at 2 GHz) between the A08 output and the filter input. Fig. 12(a)–(c) show respectively the modeled and measured conversion gains, and fundamental and third harmonic rejection responses of this design for a 25 mA bias and 0 dBm input power. Slightly more than 0 dB conversion gain was obtained with this design for frequencies between 3.75 and 4.22 GHz, and the fundamental and third harmonic outputs were both more than 40 dB below the desired second harmonic output. This design allowed for no margin with regard to stability between 2.5 and 3.0 GHz. A more practical design would employ a shorter length of transmission line between the A08 and the edge-coupled filter to guarantee stability at the expense of about 0.5 dB less conversion gain.

Another medium band design was developed utilizing the above output network and an elliptic function lowpass input network [20] to reflect harmonic signals back into the base of the A08. The objective of this design was to assess the effect of input "reflector networks" on the

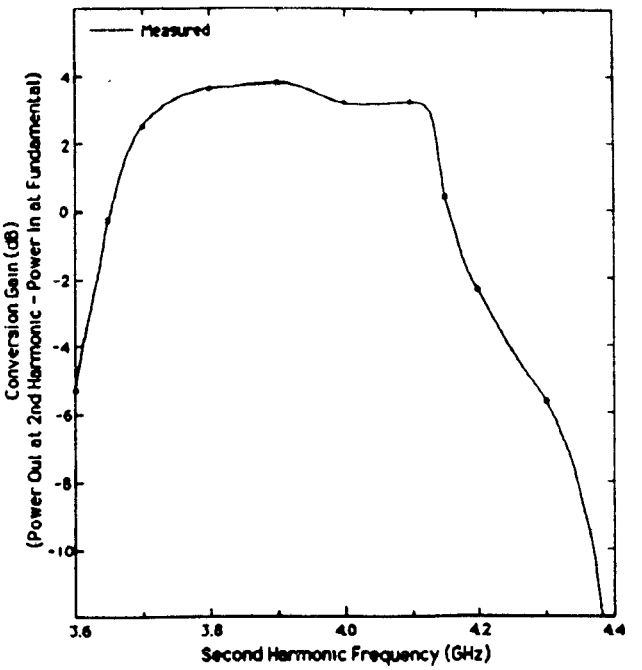

Fig. 13. Measured conversion gain of medium band design #2. Bias = 15 mA; input power = 0 dBm.

doubler conversion gain. Fig. 13 shows a plot of the resultant conversion gain for a bias current of 15 mA. The results of an additional design are presented in Fig. 14(a). The objective of this design was to achieve a high gain narrowband doubler by employing a circuit with the previously developed output network and a single stub input reflector circuit optimized for maximum conversion gain. This design is seen to achieve a conversion gain of 7 dB by optimizing the distance between the input reflector network and the A08 device input. The positive used to fabricate this design is shown in Fig. 14(b). These results clearly indicate that the addition of the reflective input network leads to an improvement in conversion gain performance.

Wide Bandwidth Designs

A broader bandwidth (40%) doubler design has been realized by synthesizing a different type of edge-coupled output network [21]. This topology, capable of realizing octave bandwidth, provides a stable, although suboptimum (in terms of conversion gain) output termination for the active device. A simple single stub network has been included on the input of the 40% bandwidth design to improve input SWR. Measured and modeled results for this design are shown in Fig. 15 where it is seen that a very flat conversion gain of 0 dB is achieved and fundamental and third harmonic rejections are greater than 30 dBc. Note that in Fig. 15, fundamental, second harmonic and third harmonic responses are all plotted on the same graph and that the horizontal scale must be multiplied by the appropriate factor (e.g., the scale reads 3–5 GHz for the second harmonic).

(a)

(b)

Fig. 14. (a) Medium band high gain design. (b) Positive for the 7 dB device.

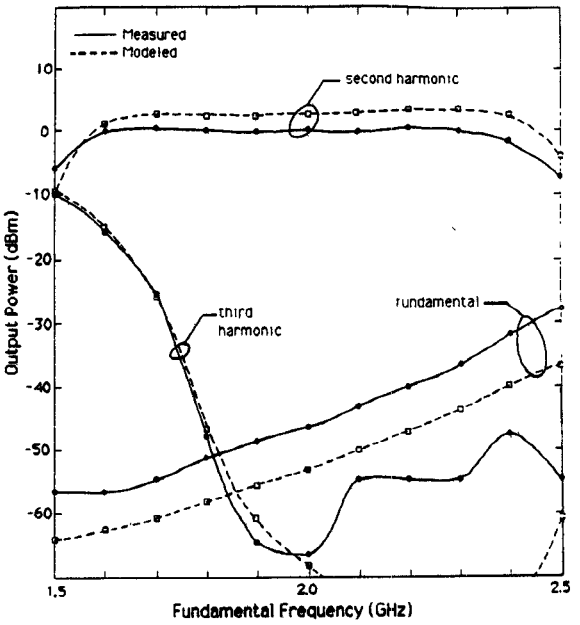

Fig. 15. Measured and modeled output power of wide-band doubler circuit (input power = 0 dBm).

V. Conclusion

Systematic techniques for design of MIC bipolar doublers have been presented. The results are unique in that excellent performance has been achieved in conversion gain, bandwidth and spectral purity. Gains of up to 7 dB have been obtained for narrowband performance ($\approx 8\%$) and approximately 0 dB for wideband performance (40%) while fundamental and higher harmonic rejections of 40 dBc have been achieved.

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